ABSTRACT

A method of fabricating a flash memory device including an array of split gate cells, comprising the steps of: providing a silicon substrate having a top surface; implanting ions into a predefined area of the substrate to form a common source region of the substrate; forming at least one floating gate over the substrate, each floating gate being associated with one of the cells and having a portion which overlies a portion of the common source region, the overlying portion of each floating gate providing for a high coupling ratio for the associated flash cell; forming a select gate over at least a portion of each floating gate; and forming a drain region associated with each cell. The high coupling ratio flash cell device of the present invention overcomes limitations associated with conventionally formed split gate flash cells by forming the common source region first and then forming the floating gates over the common source region in order to provide a high coupling ratio for the cells.